REMARKS

The foregoing amendment is to impart greater clarity and definiteness to the claims rather than to avoid prior art.

Applicants respectfully request reconsideration of this application as amended. Claims 1-39 are pending in the application. Claims 1-39 are rejected. Claims 1, 6, 10, 12, 15, 22, 24, 28, 30 and 36 are amended.

The Office Action objected to the drawings, indicating that in Figure 7B operation 740 data is shown as shifted to the "left." Applicant respectfully intends that with regard to bitstream 710, the destination buffer data has been shifted right and the shift count specified is intended to indicate an amount for that right shifting. This is in accordance, for example, with the interpretation given with regard to Figure 4A.

With regard to Claims 12, 22, 28 and 36, Office Action similarly indicates that "right" should be "left." As indicated above, Applicant respectfully intends to claim in the instant claims that the specified shift count is indicative of a right shift with regard to the right end of the second data block.

Rejections under 35 U.S.C. 102

Claims 1-39 are rejected under 35 U.S.C. 102(e), as allegedly being anticipated by Claim 1 of US Patent 6,781,589 (Macy). Applicant respectfully disagrees.

Claim 1, for example, sets forth:

> 1. (Currently Amended) A method comprising:
> determining whether any unprocessed data bits for a partial variable length symbol exist in a first data block; and
> performing a shift merge operation responsive to a shift merge instruction specifying the first data block, a second data block and a shift count, the shift merge operation to merge said unprocessed data bits from said first data block with said second data block, wherein a merged data block is formed.

Applicant respectfully submits that Claim 1 of Macy does not claim performing a shift merge operation responsive to a shift merge instruction specifying the first data block, a second data block and a shift count as set forth by Claim 1 of the present application as amended.

Applicant respectfully submits that that in order for a rejection based on anticipation to be made, the identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Accordingly, Applicant respectfully submits that the claims in the present application are not anticipated by Claim 1 of Macy as indicated by the Office Action.

Rejections under 35 U.S.C. 101

Claims 1-29 are rejected under 35 U.S.C. 101, as allegedly being directed to non-statutory subject matter. Applicant respectfully disagrees.

Claim 24, for example, sets forth:

> 24. (Currently Amended) An article comprising a tangible machine readable medium that stores a program, said program being executable by a machine to perform a method comprising:
> determining whether any unprocessed data bits for a partial variable length symbol exist in a first data block; and
> performing a shift merge operation responsive to a shift merge instruction specifying the first data block, a second data block and a shift count, the shift merge operation to merge said unprocessed data bits from said first data block with said second data block, wherein a merged data block is formed.

An analysis of the instant claims must be performed in order to make a determination of whether the subject matter is statutory. Such analysis should correlate each claim element with corresponding structures, materials or acts set forth in the specification.

The Federal Circuit makes it clear that the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention. "The person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Phillips v. AWH Corp.*, 415 F.3d at 1313.

Applicant respectfully submits that the claimed performing a shift merge operation responsive to a shift merge instruction specifying the first data block, a second data block and a shift count, the shift merge operation to merge said unprocessed data bits from said first data block with said second data block, wherein a merged data block is formed, as set forth in Claim 24 (and also in Claims 1 and 15), would not be treated merely as a program per se by a person of skill in the art in the context of the entire patent.

The instant language when correlated with the corresponding structures and processes set forth in the specification makes it apparent to one of skill in the art that the claimed invention has a practical application in the technical arts, i.e. to improve the performance of variable length encoding (VLC) and decoding (VLD) such as are found in image and video processing tasks, and in communications, and in various compression techniques and standards, e.g. JPEG and MPEG.

In addition, Applicant respectfully submits, that the present application clearly asserts such a practical application in the technical arts.

For example, paragraphs 33-34 of the specification (emphasis added) asserts that:

> Applications of coding and decoding operations are found in a wider array of image and video processing tasks and communications. One example of coding/decoding algorithms is used in processing of Motion Picture Expert Group (MPEG) video. Variable length encoding (VLC) and decoding (VLD) are used in various compression techniques and standards such as JPEG and MPEG. In variable length codes, the different symbols require a different numbers of bits. One operation in variable length decoding is to extract bits out of the bitstream before decoding the symbols. In order to extract a variable number of bits from

> the bitstream for a variable length symbol, the beginning of symbols have to be addressed by bits instead of bytes. However, addressing memory on a bit-wise level is difficult, data from the bitstream is sent to a temporary register first. The bits are then shifted around and manipulated to emulate bit addressability of the bitstream.
>
> Unfortunately, current methods and instructions target the general needs of variable length coding/decoding and are not comprehensive. In fact, many architectures do not support a means for efficient extraction of varying length data symbols. In addition, data ordering within data storage devices such as SIMD registers, as well as a capability of merging values in a register and for partial data transfers between registers, are generally not supported. As a result, current architectures require unnecessary data type changes which increases the number of clock cycles required to order data for arithmetic operations. A SIMD shift merge instruction can be useful in audio and video applications where large amounts of packed data are processed. For example, a single shift merge instruction of one embodiment is capable of replacing multiple instructions that would be needed to perform an equivalent data manipulation. By reducing the number of instructions needed, throughput can be increased and processing resources such as registers and execution units freed up.

Thus the specification makes it readily apparent to one of skill in the art that the claimed invention has a practical application in the technical arts.

The Supreme Court held that the focus in any statutory subject matter analysis be on the claim as a whole, stating "When a claim containing a mathematical formula implements or applies that formula in a structure or process which, when considered as a whole, is performing a function which the patent laws were designed to protect (e.g., transforming or reducing an article to a different state or thing, then the claim satisfies the requirements of § 101." *In re Alappat*, 33 F.3d 1526, 1543 (Fed. Cir. 1994) (quoting *Diehr*, 450 U.S. at 192, 209 USPQ at 10).

This notion is sometimes phrased in terms of requiring a transformation or reduction of 'subject matter.' In Schrader, the phrase 'subject matter' was determined not to be limited to tangible articles or objects, but includes intangible subject matter, such as data or signals, representative of or constituting physical activity or objects. *Schrader*, 22 F.3d at 295, 30 USPQ2D (BNA) at 1459.

Thus Applicant respectfully submits that Claims 1-29 are directed to statutory subject matter.

CONCLUSION

Applicants respectfully submit the amended specification, the amended drawings, and the present claims for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Lawrence Mennemeier at (408) 765-2194.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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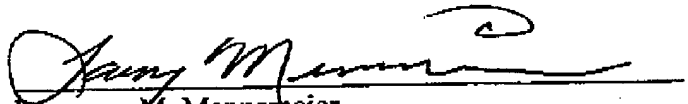

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